

**Notice of References Cited**

Application/Control No.

10/023,117

Applicant(s)/Patent Under

Reexamination

DE OLIVEIRA KASTRUP PEREI

Examiner

Richard Ellis

Art Unit

2183

Page 1 of 1

**U.S. PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-5,321,845 A	06-1994	Sawase et al.	712/37
	B	US-4,346,438	08-1982	Potash et al.	712/209
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

**FOREIGN PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Hauck, Scott, Fry, Thomas W., Hosler, Matthew M., Kao, Jeffrey P., The Chimaera Reconfigurable Functional Unit, The 5th Annual IEEE Symposium on FPGAs for Custom Computing Machines, April 16-18, 1997.
	V	Hutchings, Brad L., Wirthlin, Michael J., Implementation Approaches for Reconfigurable Logic Applications, Proceedings of the 5th International Workshop on Field Programmable Logic and Applications, Oxford, UK, August 29-September 1, 1995.
	W	Razdan, Rahul, Smith, Michael D., A High-Performance Microarchitecture with Hardware-Programmable Functional Units, Proceedings of the 27th Annual International Symposium on Microarchitecture, November 30-December 2, 1994.
	X	

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.